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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/870,767	06/01/2001	Richard S. Norman	13691	1309

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EXAMINER	
NGUYEN, SON XUAN	
ART UNIT	PAPER NUMBER
2664	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/870,767	NORMAN ET AL.
	Examiner	Art Unit
	SON X. NGUYEN	2664

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 33-36* is/are rejected.

7)☒ Claim(s) *14-32 and 37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 34 is objected to because of the following informalities:

This claim does not depend on claim 5. It depends on claim 4. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-8 are rejected under 35 U.S.C. 102(e) as being participated by Prasad at al (U.S 6,275,491), hereinafter referred to as Prasad.

Regarding claim 1, Prasad discloses a switch fabric implemented on a chip, comprising:

a) An array of cells (port processors of Figure 2);

b) An I/O interface (port interfaces of Figure 2) in communication with said array of cells for permitting exchange of data packets between said array of cells and components external to said array of cells;

c) Each cell communicating with at least one other cell of said array, permitting: I) exchange of data packets between the cells of said array; II) exchange of control information between the cells of said array (data buses DB1 to DB4 of Figure 2);

d) Each cell operative to control transmission of data packets to other cells of said array at least in part on a basis of the control information (port processor control bus PPCBUS of Figure 2).

Regarding claim 2, Prasad discloses array of cells includes: a) a plurality of data channels for transporting data packets between the cells of said array (data buses DB1 to DB4 of Figure 2); and b) a plurality of channels distinct from said data channels for conveying the control information to the cells of said array (port processor control bus PPCBUS of Figure 2).

Regarding claim 3, Prasad discloses each of the channels of the plurality of channels distinct from said data channels interconnects two cells of said array (PPCBUS of Figure 2).

Regarding claim 4, Prasad discloses each cell of said array includes: a) a transmitter in communication with said I/O interface and in communication with every other cell of said array, said transmitter operative to process a data packet received from said I/O interface to determine a destination of the data packet and forward the data packet to at least one cell of said array selected on a basis of the determined destination (FS XMIT 36 and XMIT 48 of Figure 3); b) a plurality of receivers associated with respective cells of said array, each receiver being in communication with a respective cell allowing the respective cell to forward data packets to the receiver (FS RCVR 46 and RCVR 32 of Figure 3); c) said receivers (RCVR 32 of Figure 3) in communication with said I/O interface for releasing data packets to said I/O interface.

Regarding claim 5, Prasad discloses each data channel of said plurality of data channels is associated with a given cell of said array, the data channel associated with said given cell connecting the transmitter of said given cell to receivers in cells other than said given cell and associated with said given cell (data buses DB1 to DB4 of Figure 2 and 3).

Regarding claim 6, Prasad discloses each data channel of said plurality of data channels is associated with a given cell of said array, the data channel associated with said given cell connecting the transmitter of said given cell to a receiver in every cell of said array of cells and associated with said given cell (data buses DB1 of Figure 2 and 3).

Regarding claim 7, Prasad discloses the plurality of data channels are independent from one another, wherein transmission of a data packet over one data

channel is made independently of transmission of a data packet over another data channel (lines 14-23 of column 5).

Regarding claim 8, Prasad discloses each data channel performs a parallel data transfer (lines 65-68 of column 7).

Regarding claim 33, Prasad discloses each cell further including a central processing unit (CPU) (VPCI translator/arbiter 38 of Figure 3) connected to the transmitter, said transmitter being further operative to process a data packet received from said CPU to determine a destination of the data packet and forward the data packet to at least one cell of said array selected on the basis of the determined destination.

Regarding claim 34, Prasad discloses each cell further including a central processing unit (CPU) (VPCI translator/arbiter 38 of Figure 3) connected to the transmitter, said transmitter being further operative to process a data packet received from said CPU to determine a destination of the data packet and forward the data packet to at least one cell of said array selected on the basis of the determined destination, wherein data packets received by the transmitter in a given cell from the I/O interface and from the CPU in said given cell share the data channel associated with said given cell (lines 2-7 and lines 13-20 of column 8).

Regarding claim 35, Prasad discloses each cell further including a central processing unit (CPU) (VPCI translator/arbiter 38 of Figure 3) connected to the plurality of receivers, said receivers being further operative to determine whether data packets

are to be released to the I/O interface or to the CPU and release said data packets accordingly (lines 65-68 of column 7 and lines 1-4 of column 8).

Regarding claim 36, Prasad discloses each data packet comprises a field indicative of whether the data packet is destined for a CPU and wherein said receivers are operative to determine whether data packets are to be released to the I/O interface or to the CPU on the basis of said field (routing label of incoming cell; and data packet inherent containing a field for destination).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 9, 10, 11, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prasad at al (U.S 6,275,491), and further in view of Masaaki (U.S 6,438,143).

Regarding claims 9 and 10, Prasad discloses the transmitter of said given cell.

Prasad, however, fails to disclose the transmitter includes a memory for storing data packets received from said I/O interface, said memory includes a plurality of segments, each segment being associated with a receiver in a cell of said array to

which the transmitter of said given cell is capable of forwarding a data packet via a data channel from said plurality of data channels.

Masaaki teaches the transmitter includes a memory for storing data packets received from said I/O interface (lines 34-36 of column 3), said memory includes a plurality of segments (lines 5-6 of column 14), each segment being associated with a receiver in a cell of said array to which the transmitter of said given cell is capable of forwarding a data packet via a data channel from said plurality of data channels (Figure 7).

It would have been obvious to one ordinary skill in the art at the time the invention was made to modify Prasad's method to incorporate a setup where transmitter includes a memory and memory includes a plurality of segments, the motivation being that using transmitter including a memory and memory including a plurality of segments would be capable of forwarding a data packet to correct destination.

Regarding claims 11 and 12 Prasad discloses the transmitter of said given cell.

Prasad, however, fails to disclose the transmitter includes a control entity, said control entity being operative to process a data packet forwarded from said I/O interface to determine a cell of said array to which the data packet is destined and identify on a basis of the determined cell a segment of said memory in which the packet is to be loaded; and fails to disclose said control entity includes a plurality of queue controllers associated with respective segments of said memory.

Masaaki teaches the transmitter includes a control entity (lines 34-36 of column 3), said control entity being operative to process a data packet forwarded from said I/O

interface to determine a cell of said array to which the data packet is destined and identify on a basis of the determined cell a segment of said memory in which the packet is to be loaded (lines 36-37 of column 3); and teaches control entity includes a plurality of queue controllers associated with respective segments of said memory (lines 8-12 of column 14).

It would have been obvious to one ordinary skill in the art at the time the invention was made to modify Prasad's method to incorporate a setup where transmitter includes a control entity and control entity includes a plurality of queue controllers, the motivation being that using transmitter including a control entity and control entity including a plurality of queue controllers would process a data packet forwarded from said I/O interface to determine a cell of said array.

Regarding claim 13, Prasad discloses the transmitter of said given cell.

Prasad, however, fails to disclose the transmitter includes a memory, said memory implementing a plurality of registers, each register being associated with a queue controller and being suitable for holding data representative of a degree of occupancy of a segment of said memory associated with the queue controller.

Masaaki teaches the transmitter the transmitter includes a memory, said memory implementing a plurality of registers (lines 5-6 of column 14), each register being associated with a queue controller and being suitable for holding data representative of a degree of occupancy of a segment of said memory associated with the queue controller (lines 8-12 of column 14).

It would have been obvious to one ordinary skill in the art at the time the invention was made to modify Prasad's method to incorporate a setup where transmitter includes a memory and memory implementing a plurality of registers, the motivation being that using transmitter including a memory and memory including a plurality of registers, each register being associated with a queue controller would be capable of representative a degree of occupancy of a segment of said memory associated with the queue controller.

Allowable Subject Matter

6. Claims 14-32, 37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Higashida, Masaaki (U.S 6,438,143), Image packet communications system.

b) Epps et al. (U.S 6,8132,243), High-speed hardware implementation of red congestion control algorithm.

c) Ofek, Yoram (U.S 6,760,328), Scheduling with different time intervals.

d) Ofek, Yoram (U.S 6,757,282), Fast switching of data packet with common time reference.

e) Miles et al. (U.S 6,665,495), Non-blocking, scalable optical router architecture and method for routing optical traffic.

d) Mussman et al. (U.S 6,188,687) Broadband switch that manages traffic and method therefor.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SON X. NGUYEN whose telephone number is 571-272-3139. The examiner can normally be reached on 8 AM -5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RICKY NGO
PRIMARY EXAMINER
11/14/04